Scalable Graphite/Copper Bishell Composite for High-Performance Interconnects

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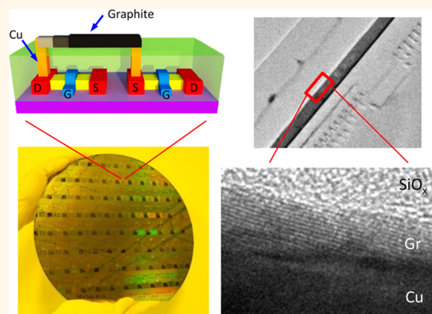
ABSTRACT We present the fabrication and characterizations of novel electrical interconnect test lines made of a Cu/graphite bishell composite with the graphite cap layer grown by electron cyclotron resonance chemical vapor deposition. Through this technique, conformal multilayer graphene can be formed on the predeposited Cu interconnects under CMOS-friendly conditions. The low-temperature (400 °C) deposition also renders the process unlimitedly scalable. The graphite layer can boost the current-carrying capacity of the composite structure to 10^8 A/cm^2, more than an order of magnitude higher than that of bare metal lines, and reduces resistivity of fine test lines by ∼10%. Raman measurements reveal that physical breakdown occurs at ∼680−720 °C. Modeling the current *vs* voltage curves up to breakdown shows that the maximum current density of the composites is limited by self-heating of the graphite, suggesting the strong roles of phonon scattering at high fields and highlighting the significance of a metal counterpart for enhanced thermal dissipation.



KEYWORDS: graphene · interconnect · chemical vapor deposition · low temperature

The rapid evolution of integration technology in semiconductor electronic devices has resulted in a significant increase in device density and speed, and this trend is expected to continue in the near future, leading to an increasing number of wires within a finite chip area, thus forcing an aggressive shrinking of interconnect pitch, even at the global level. The *RC* delay of Cu interconnects is expected to grow due to the increasing resistance caused by the reduced cross-section of the wires, as well as increasing parasitic capacitance due to the reduced interconnect pitch. Various potential solutions, including the use of new materials such as carbon nanostructures, low-κ dielectrics, impurity doping in Cu, and different liners in damascene structures, have been proposed to alleviate this problem.[1−7]

One of the most difficult challenges for interconnects is the introduction of new materials that meet the wire conductivity requirements and reduce dielectric permittivity. Replacement or improvement of the current Cu interconnects is becoming imminent as line widths continue to shrink. In this context, graphene (or graphite) has emerged as the prime material of choice for interconnects due to its low resistivity and susceptibility to high current density.[8,9] Previous reports show that exfoliated few-layer graphene exhibits a current-carrying capacity of 10^9 A/cm^2, 3 orders of magnitude higher than that of copper at the same dimensions.[10,11] Recently, multilayer graphene has been proved to be an excellent capping material for Cu interconnects by improving the reliability of the interconnect structure.[12−14] However, using graphene layers as interconnects requires a process suitable for mass production that allows for the deposition on the patterned structures. A number of approaches have been reported for graphene synthesis, among which chemical vapor deposition (CVD) can best integrate with current semiconductor manufacturing technologies and meet the quality requirements.[15−17] For example, CVD growth of mono- to multilayer graphene films has been demonstrated on Ni substrates, while uniform and large-area graphene films can

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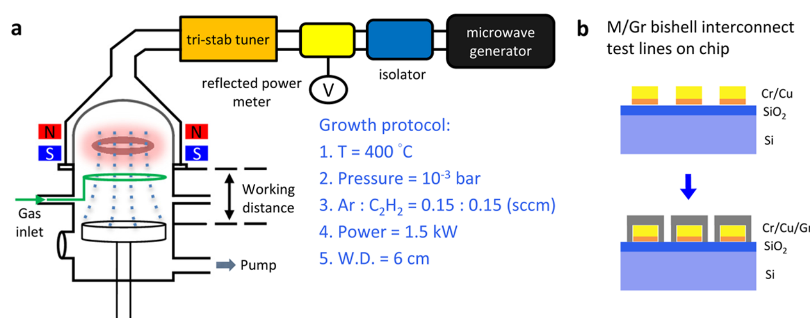

Figure 1. (a) Schematic illustration of a homemade ECR-CVD system and growth parameters for graphite deposition on predefined Cr/Cu metal lines used in the current study. (b) Simple process flow and schematic illustrations of the test line cross-section.

be readily produced on Cu foils under a well-controlled gas atmosphere.[17,18] The growth temperature typically spans the range 950−1050 °C for Cu and 800−900 °C for Ni. The high-temperature process makes the direct deposition of graphene layers in the CMOS back-end wiring infeasible. Considerable effort has been devoted to developing diverse approaches to synthesize graphene at reduced temperatures. Recently, Sun *et al.* showed that a continuous graphene film can be obtained through the thermal annealing of poly(methyl methacrylate) (PMMA) at 800 °C.[19] Li *et al.* later demonstrated that the growth temperature can be substantially lowered to 300 °C using benzene as a carbon feedstock. In the latter case, only small graphene flakes are formed on the Cu substrate.[20] A number of growth methods using radiofrequency or microwave plasmas have also been reported.[21−23] However, the typical growth temperature remains as high as 600−800 °C due to the trade-off between the graphene crystallinity and growth temperature.

In this paper, we show the growth of multilayer graphene (graphite) on Cu lines using electron cyclotron resonance CVD (ECR-CVD) at 400 °C, forming a metal/graphite (M/Gr) bishell structure as interconnects. Through this technique we are able to break the self-limiting growth constraint in the CVD process and deposit a thick graphitic film on Cu lines at a temperature harmless to the existing field-effect transistors. The graphite thickness is found to be linearly proportional to the growth time in the early stage of the deposition and can be controlled at an accuracy of ±2 nm in the thickness range of 0−10 nm, calibrated using light transmittance of graphite films transferred from Cu foil to glass (Supporting Information, Figure S2). The growth rate deviates slowly from this linearity as the film thickness further increases. The standard four-probe method has been adopted throughout the electrical measurements in this work, with measurement configuration shown in the Supporting Information (Figure S9). In the electrical measurements, we show that the graphitic overcoat not only reduces the resistivity of M/Gr composite lines but also increases the maximum current density up to 10^8 A/cm^2, a value 1−2 orders of magnitude above the sustainable limit of typical metal interconnects. The M/Gr composite features the following properties in processing: (i) one-step (nontransfer) and selective deposition of graphite on metal lines, (ii) conformal passivation overcoat, and (iii) low thermal load.

RESULTS AND DISCUSSION

Figure 1a shows the experimental setup and a typical protocol for low-temperature graphite deposition on Cu. It has been shown in our previous ECR-CVD study that a nanographene film can be formed on silicon oxide due to the nucleation of SiC clusters.[24] The growth of nanographene films can be suppressed with the aid of hydrogen addition. However, excess hydrogen may also deteriorate the graphite grown on metal lines due to the etching effect of hydrogen radicals.[25] It should be noted that the ECR-CVD graphene layers grown on metal substrates such as Cu, Ni, and CuNi alloys (Supporting Information Figure S1 and S2) exhibit a much better crystallinity than the best graphene layers directly grown on typical oxides (amorphous silicon oxides, quartz, TiO_2, and sapphire) (Supporting Information Figure S3). Therefore, comparing the electrical properties of M/Gr composite lines with that of bare Gr lines is not justified. Figure 1b shows two types of test lines used in the current study. The first type is metal (control) lines made of Cr(10 nm)/Cu(t_{Cu} nm), and the other is composite lines with an additional graphite layer on top, Cr(10 nm)/Cu(t_{Cu} nm)/Gr(t_{Gr} nm). The thin Cr layer acts as a liner. It is used to enhance the adhesion between Cu and the SiO_2/Si substrate and also act as a diffusion barrier of Cu to improve metalization reliability. The graphite thickness t_{Gr} varies from 10 to 45 nm while keeping metal thickness constant. For electrical measurements, the control lines were additionally annealed under the conditions identical to the ECR-CVD process so as to obtain comparable metal grain sizes in both types of lines. Confocal Raman spectroscopy and transport measurements of back-gated FETs were used to access the quality of ECR-CVD graphene, with data provided in the Supporting Information (Figure S1, S4, S5).

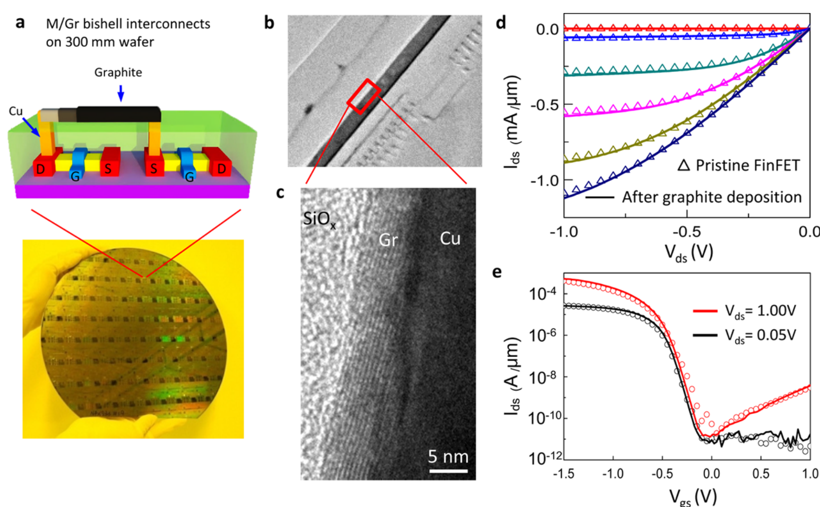

Figure 2. Direct deposition of graphite layers on state-of-the-art Cu interconnects. (a) Schematic and pictorial illustrations of the architecture of Cu/Gr composite interconnects formed above FinFETs on a 300 mm Si wafer. (b) Low-magnification of a TEM image showing the Metal 1 (Cu) interconnect on top of a series of p-type FinFETs that possess a gate length of 22 nm. (c) Locally zoomed TEM image of (a). The periodic thin lines correspond to 12−15-layer stacks of graphene. The top SiO_x is deposited to protect the Cu/Gr structure when slicing samples for TEM measurements. (d) Comparison of output characteristics of a pMOS FinFET before and after graphite deposition. The gate voltage was swept from 0 to −1.5 V with a step of −0.25 V. (e) Comparison of transfer characteristics of the same pMOS FinFET before (circles) and after (solid lines) graphite deposition.

We applied this low-temperature growth method to deposit a graphite layer on state-of-the-art Cu interconnects atop pMOS FinFETs, as schematically shown in Figure 2a. The FinFETs were fabricated using 22 nm technology node integration flow on a 300 mm Si wafer. Only one level of Cu interconnects (Metal 1) was made above the transistors. Figure 2b and c show the cross-section of transmission electron microscopy (TEM) images of the M/Gr bishell. The low-temperature process prevents granulation and diffusion of copper, keeping the structure intact after the back-end manufacturing processes. Figure 2d compares the output characteristics of a pMOS FinFET before and after the graphite deposition. The finite thermal load and mild growth conditions ensure no apparent deterioration of the transistor properties after graphite deposition. Only a slight increase of the on-state current is seen, presumably due to the lowering of contact resistance during the growth. Figure 2e shows the transfer characteristics of the same device. For the low drain bias ($V_{ds} = 0.05$ V), the device exhibits nearly identical gated current traces before and after graphite deposition. A slight improvement of the on-state current and subthreshold swing is also observed when the drain bias is increased to 1.0 V.

To gain more physical insight into the electrical properties of the M/Gr composite lines, we further measure and compare a series of composite and control lines in different dimensions. Electrical characterizations including resistivity (ρ) and current density (j) were all carried out at ∼25 °C in air. The preferred condition would be to perform the measurements in a vacuum so as to compare the practical interconnect structures that are capped with dielectrics. Figure 3 shows the line length- and width-dependent current density. The $j_{M/Gr}^{max}$, defined as the maximum current density at physical breakdown, is found to have weak dependence upon the line length, but varies noticeably with the line width, attributed to the increasing surface and boundary scatterings as the line width decreases. Aside from the size effect, $j_{M/Gr}^{max}$ is always higher than j_{M}^{max} at the same line width by an order of magnitude.

The inset of Figure 3b shows the histogram of resistivity at different line widths. A noticeable resistivity improvement can be seen in the composite lines measured, particularly for small line width, *e.g.*, a decrease of about 10% for a 200-nm-wide composite line when compared to the pure metal counterpart. This is due to the size-independent ρ_{Gr}, while ρ_M increases largely with decreasing metal grain size in the reduced line width. Given that each graphene layer has uniform resistance and is electrically connected to the underlying metal in parallel, the total resistance of the composite can be obtained through the equation

$$\frac{1}{R_{M/Gr}} = \frac{1}{R_M} + \sum_N \frac{1}{R_{Gr}} \qquad (1)$$

The resistivity of the composite lines is related to its geometry and written as

$$\frac{w_{M/Gr}t_{M/Gr}}{\rho_{M/Gr}} = \frac{w_M t_M}{\rho_M} + \sum_N \frac{(w_{Gr}t_{Gr} + t_M t_{Gr})}{\rho_{Gr}} \qquad (2)$$

where w is the width of the test line and $t_{M/Gr} = t_M + Nt_{Gr}$ is the total thickness of the composite. In the right-hand side of the above equation, the sidewall contribution is also taken into account in the graphite term. Then, the total

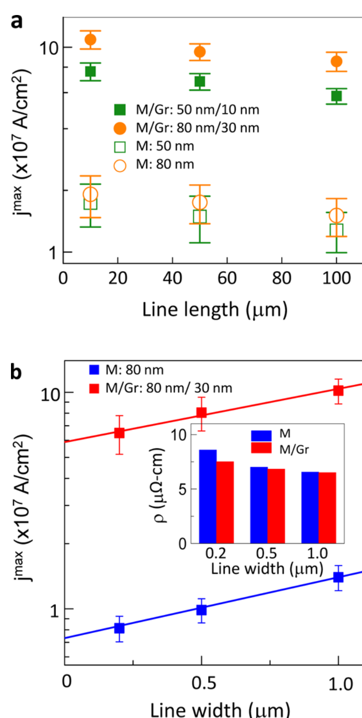

Figure 3. (a) j^{max} *vs* line length plots for the M/Gr composite and control lines. Two different t_{Gr} are compared. (b) j^{max} *vs* line width plots for the M/Gr composite and control lines. Inset shows the histogram of resistivity at different line widths, with t_{Gr} = 30 nm in the composite lines.

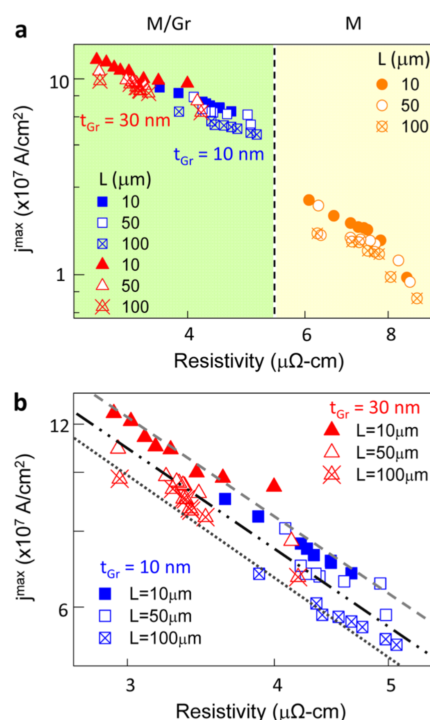

Figure 4. (a) j^{max} *vs* ρ plots for M/Gr composite and control lines with different line lengths. The line width is fixed at 2 μm. The cross-sectional areas of the composite lines are the same as those of control lines. t_{Gr} = 10 and 30 nm are compared. (b) Linear fits to the plots shown in (a) for the composite lines.

cross-sectional area of the graphite overlayer is of the form $w_{Gr}t_{Gr} + t_M t_{Gr}$. Taking the 200-nm-wide test line as an example (Figure 3b and Figures S10b and S11 in the Supporting Information), where $\rho_{M/Gr} = 7.5$ and $\rho_M = 8.5$ $\mu\Omega$ cm are acquired from measurements, we obtain $\rho_{Gr} = 6.3$ $\mu\Omega$ cm if the sidewall graphite is also taken into account in the calculation. This value is consistent with the separate measurements of isolated graphite resistivity (Supporting Information Figure S6). It indicates that the graphite cap layer starts showing its impact on the composite resistivity when $\rho_M > \rho_{Gr}$. It holds especially for a small line width where the resistive barrier layer in a damascene structure such as Ta and W starts playing a dominant role in the metal resistivity, and the electron scattering at the interface and grain boundaries becomes non-negligible. Further comparing with interconnects made of pure carbon nanotube networks, the graphite layer shows a superior property in terms of resistivity; that is, the carbon nanotube resistivity is on the order of 10^{-3} Ω cm, 3 orders of magnitude higher than graphite resistivity at similar dimensions.[26,27]

Figure 4a shows the j^{max} *vs* ρ plots of the composite and control lines. It is found that $j^{max}_{M/Gr}$ increases with the graphite thickness and reaches 10^8 A/cm^2 for the 30-nm-thick graphite coverage, an order of magnitude higher than j^{max}_M, but still lower than those obtained in mechanically exfoliated single-layer graphene ribbons.[8,9] The increase of $j^{max}_{M/Gr}$ indicates that the graphite layer provides parallel and low resistive pathways along the channel and dominates current conduction in the M/Gr composite structure. A power law, $j = A\rho^{-n}$, can be used to describe the relationship between the current density and resistivity throughout the measurements (Figure 4b). A fit to the power law yields an exponent n ranging from 0.94 to 1.24 for different line lengths, suggesting a constant breakdown electric field model with $j \propto 1/\rho$. This is essentially consistent with the wall-by-wall breakdown of multiwalled carbon nanotubes,[28] a rolled-up form of graphite.

Figure 5a shows the optical photographs of composite lines after electrical breakdown. The failures are mostly observed at a point removed from the contacts, $x \approx L/4$, irrespective of graphite thickness (from t_{Gr} = 10 to 45 nm). The breakdown of composite lines occurs as a result of oxidation of graphene layers at high fields, with joule heating being the major cause.[9] To measure the peak temperature along the channel, Raman spectra were taken on different positions of the channel at different electrical powers, and *G* peak shifts with respect to zero bias were used to extract the temperature (Figure 5b). Figure 5c shows the *G* peak position as a function of electrical power. The frequency decreases sharply with increasing electrical power, indicating that the Joule heating is responsible for phonon softening. Temperature-dependent measurements of graphene *G* mode have shown that its frequency decreases linearly with temperature.[8,29] This allows us to calculate the coarse

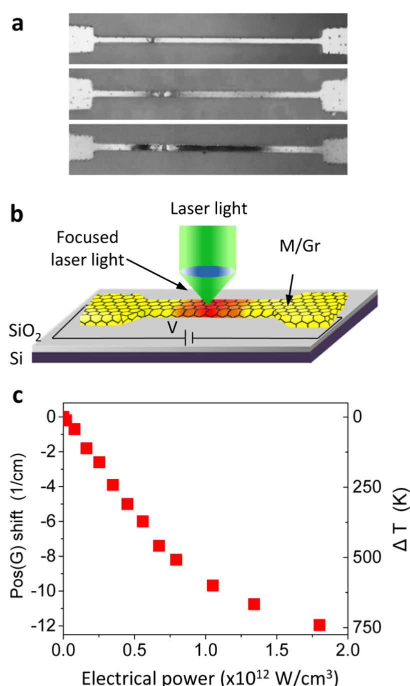

Figure 5. (a) Optical photographs of the failure spot for the composite lines with t_{Gr} = 10 nm (top), 22 nm (middle), and 32 nm (bottom). (b) Schematic illustration of temperature measurements along the composite channel using Raman spectroscopy. The power, which is locally produced by Joule heating, varies proportionally to the corresponding local resistance R as I^2R, where I is the current flowing through the test structure. To estimate the local temperature of the channel under different bias voltages, G peak shifts with respect to that at zero bias were recorded. (c) G peak shifts as a function of electrical power at the hot spot of a composite channel with $t_{Gr} \approx 10$ nm.

temperature profiles along our composite channel using the temperature coefficient $\chi = -0.016$ cm^{-1}/°C extracted from exfoliated graphene.[29,30] Typical breakdown temperature of our composite lines is at ~680–720 °C, higher than those observed in exfoliated graphene nanoribbons and single-walled carbon nanotubes lying on a SiO_2 substrate (~600 °C).[9,31,32]

Figure 6 shows the $j-V_{ds}$ curves for different graphite thicknesses, measured in air. In these measurements, the voltage was swept up continuously until breakdown occurs. In each curve, the current is initially linear but starts saturating at an increasing bias. The saturation implies an increasing electron–phonon scattering in graphite, resulting in self-heating, resembling the nonlinear $I-V_{ds}$ curves of graphene ribbons at high fields.[8,9] The breakdown current density increases with the graphite thickness (Figure 6b). At t_{Gr} > 30 nm (Gr-to-M ratio >0.15), the M/Gr composite can withstand a total current density of $(1.2-1.5) \times 10^8$ A/cm^2, while the bare metal line is already damaged at $j_M^{max} \approx 1.1 \times 10^7$ A/cm^2. This result verifies that the graphite cap layer dominates the current conduction and alleviates electromigration of the underlying Cu wire. The composite structure has significantly boosted the electrical properties compared with the bare metal counterpart. In the analysis of the above breakdown behavior, we also found that the breakdown occurs at a nearly constant power density of $(1-2) \times 10^{12}$ W/cm^3 for different graphite thicknesses (t_{Gr} = 10–45 nm) with the same metal dimensions (Figure 6c), indicating a uniform quality of the graphene layers grown by ECR-CVD on Cu. In comparison with exfoliated graphene ribbons on SiO_2/Si,[8,9] higher breakdown powers of ~6×10^{12} and $(10-30) \times 10^{12}$ W/cm^3 (both measured in air) were reported. This finding shows that breakdown is strongly correlated to the defect density and there is room to improve our graphite quality for future applications.

To look into the breakdown mechanism of the composite, we model the $j-V_{ds}$ curves using the developed finite element simulation.[33] At high fields, it is justified to consider only the graphite contribution to the current density in the M/Gr composites because of $j_{M/Gr} \gg j_M$ at the same t_M and V_{ds}.[34] Electron mobility of 250 cm^2/V·s and contact resistance of 188 Ω extracted from Figure S4 in the Supporting Information were used for our calculations. The current density j is a function of applied bias V_{ds} and temperature T:

$$j = \frac{qV_{ds}}{t}\left[\int_0^L \frac{\varepsilon_x}{n(T_x)v_{Gr}(\varepsilon_x, T_x)}\,dx\right]^{-1} \quad (3)$$

where q is the elementary charge, x is the coordinate along the graphite channel, n is the carrier density at location x, T_x is the absolute temperature at location x, $\varepsilon_x = -dV_x/dx$ is the electric field, and v_{Gr} is the drift velocity in graphite.[9] At the onset of nonlinear behavior (V_{ds} > 0.3 V) shown in Figure 6, $n(T_x)$ in the graphite channel becomes dominated by thermally generated carriers (electrons and holes). The carrier density at different bias voltages can be calculated through the equation $2n(T_x) = 2(\pi/6)((k_BT_x)/(\hbar v_F))^2$ in this regime, where k_B is the Boltzmann constant, $\hbar$ is the reduced Planck constant, $v_F \approx 10^8$ cm/s is the Fermi velocity, and T_x is calculated from the heat diffusion equation (Methods), with the maximum temperature extracted from the Raman G shift upon voltage applied (Figure 5c). In eq 3, the drift velocity is a function of electric field and temperature and typically described by the empirical equation $v_{Gr}(\varepsilon_x, T_x) = v_{sat}[1 + (\varepsilon/\varepsilon_c)^\gamma]^{-1/\gamma}$, where ε_c is the critical electric field for the onset of nonohmic behavior, and γ is a parameter. The current density in eq 3 can be solved self-consistently with the Poisson equation and the heat equation along the graphite channel. When self-heating is taken into account, simulated $j-V_{ds}$ curves and breakdown voltages (solid lines in Figure 6a) are essentially in agreement with the measured data (symbols in Figure 6a), except for a little downshift of the simulated $j-V_{ds}$ curves owing to the exclusion of metal heat conduction in the calculation. This result is consistent with the constant breakdown field found in the current density *vs* resistivity relationship discussed above and also with the mechanism governing

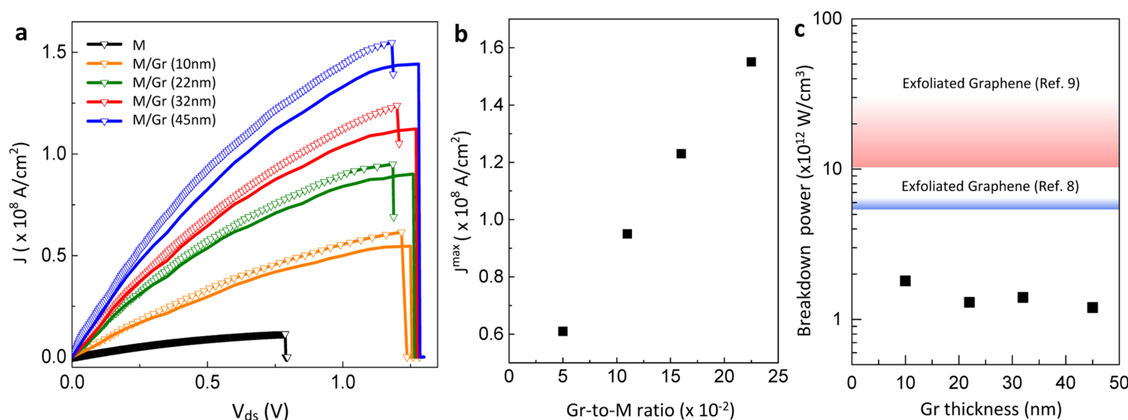

Figure 6. (a) Measured (symbols) and simulated (lines) current density *vs* bias voltage up to breakdown of composite and control lines, with line width of 200 nm, thickness of 200 nm, and length of 10 μm. Different thicknesses of the graphite cap are indicated. (b) j^{max} *vs* Gr-to-M ratio for the composite lines shown in (a). (c) Comparison of breakdown power of the M/Gr composite lines shown in (a) with reported values.

the breakdown in mechanically exfoliated graphene ribbons.[8,9] It should be noted that the simulation supports the t_{Gr}-independent breakdown in the sense that each graphene layer in the graphite cap is of similar quality in electrical and thermal transport. Recently, Dorgan *et al.* showed that graphene ribbons with high electron mobility (high quality) exhibit current saturation in the $j-V_{ds}$ curves and reach j^{max} at a lower field, while more disordered graphene ribbons (low quality) show superlinear $j-V_{ds}$ characteristics with j^{max} at a higher field.[35] The t_{Gr}-independent breakdown observed in our measurements therefore indicates a uniform quality of each graphene layer grown in the graphite cap.

CONCLUSIONS

In conclusion, metal/graphite bishell interconnects have been fabricated using ECR-CVD growth of a conformal graphite film on Cu at 400 °C, and their electrical properties have been benchmarked against those of bare metal lines as providing higher current density, higher breakdown voltage, and lower resistivity. The deposition process is one-step (nontransfer), selective, and scalable. This CMOS-compatible approach paves the way for few-layer graphene or thick graphite applications in electrical interconnects that meet the requirements for low-temperature processing or flexibility.

METHODS

Deposition of Cu and Graphite. Except the Cu interconnects made on the 300 mm wafer, the Cu test lines on small silicon chips (4 cm × 4 cm) were fabricated using standard e-beam lithography with PMMA as a resist. Test line patterns with the following dimensions were created: *w* (width) = 0.2, 0.5, and 1.0 μm; *l* (length) = 10, 50, and 100 μm. Two-layer metal structure was deposited using thermal evaporator at a background pressure of 2×10^{-6} Torr. A 10-nm-thick Cr film was first deposited as the adhesion layer, so that the Cu layer stays conformally unchanged during the ECR-CVD growth of graphite at 400 °C for a couple of minutes. After a lift-off process in acetone, the samples were mounted into the ECR-CVD chamber. Graphite deposition on Cu was then carried out at a background pressure of 1×10^{-6} Torr. To clean up the Cu surface, hydrogen was introduced at a rate of 5 sccm, and the plasma was ignited at a partial pressure of 3×10^{-6} Torr at 400 W for 5 min. Then, argon and ethylene flows were open (Ar: 0.12 sccm/C_2H_4: 0.12 sccm), and the plasma was ignited at 800 W for the desired growth time, which linearly depends on the film thickness. During the growth, a low concentration of hydrogen (0.15−5 sccm, depending on graphite thickness) was added so as to suppress the direct deposition of nanographene on the bare SiO_2. After the growth, the temperature was ramped down slowly, with a constant hydrogen flow at a partial pressure of 2×10^{-4} Torr. The same growth conditions were applied to single-layer growth on Cu foil (25 μm) so as to better characterize electrical properties of the graphite layer on Cu.

Electrical Characterization of ECR-CVD Graphene. To characterize single-layer ECR-CVD graphene, a thin layer of polycarbonate was coated on graphene/Cu, followed by etching in HCl aqueous solution to remove the Cu substrate. The polycarbonate film, along with the attached graphene, was then transferred onto a conductive silicon substrate with 285 nm SiO_2 on top. The polycarbonate film was then removed using chloroform. Graphene FETs were made using e-beam lithography and the standard lift-off process. PMMA in a two-layer structure (996 and 120 K) was spin-coated on the graphene film, followed by baking at 130 °C for 30 min. A scanning electron microscope (JSM-840A) equipped with an e-beam writer (Elphy Quantum, Raith) was used to expose the PMMA layers, which were then developed with methyl isobutyl ketone and isopropyl alcohol in a ratio of 1:3. Metal contacts, Cr(0.5 nm)/Au(30 nm), were evaporated and lifted off in acetone at room temperature and rinsed with isopropyl alcohol. Keithley 2400 and 2000 instruments were respectively used as a current/voltage source and multimeter throughout the current−voltage measurements.

Raman Measurements of Test Line Temperature. A high-resolution micro Raman spectrometer (LabRaman 800, Horiba Jobin Yvon) equipped with a motorized sample stage was used to acquire the Raman spectra and coarse line mapping. The excitation source is a 532 nm laser (2.33 eV) with a laser power below 1 mW to avoid laser-induced heating. The laser spot size at focus was around 500 nm in diameter with a 100× objective lens.

Heat Equation along the Graphite Channel. In the self-consistent calculation of the $j-V_{ds}$ curves for different graphite thicknesses, the heat equation along the graphite channel is written as $A(\partial/\partial x)k(\partial T/\partial x) + p' - g(T - T_0) = 0$, where p' is the Joule

heating rate (in unit of watts) per unit length, $A = t_{Gr} \times L$ is the cross-sectional area, k is the thermal conductivity, g is the net heat loss rate to the substrate per unit length, and T_0 is the ambient temperature of the electrodes (*e.g.*, 300 K). The p' is expressed as $I^2(R - 2R_C)/L$, where R is the total resistance of the graphite and R_C is the contact resistance. If we assume that k is constant, the temperature profile T_x along the graphite channel is $T_x = T_0 + (p'/g)[1 - (\cosh(x/L_H)/\cosh(L/2L_H))]$, where $L_H = (kA/g)^{1/2}$ is the characteristic thermal healing length along the graphite channel. At $x = L/2$, the prefactor p'/g in the above equation reaches the maximum, and the breakdown occurs at $T_{BD} = T_0 + p'/g$. Since the breakdown temperature T_{BD} is measured from the Raman G shift upon voltage applied, we can obtain g and L_H for the heat equation along the graphite channel at each specific voltage. In addition, the breakdown voltage can be calculated through the equation $V_{BD} = gL(T_{BD} - T_0)/I_{BD}$.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Electrical transport, Raman, and AFM characterizations are given in Figures S1−S11. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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